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***What is Logic Synthesis?*** This video explains what is **logic synthesis** and why it is used for design optimization. For more

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information about our courses, ...

***Lec-15 logic synthesis - tools perspective.wmv***

***Electronics - Advanced Logic Synthesis***

***From a Finite State Machine to a Circuit*** Explanation of how a finite state machine can be translated to a digital circuit.

***S-4 | Logic Synthesis flow | RTL Synthesis flow | RTL to GDSII | Design Compiler (DC) tutorial*** This is the session-4 of RTL-to-GDSII flow series of video tutorials. In this session, we have discussed the theory and flow ...

***Digital Logic - State Tables and State Diagrams*** This is one of a series of videos where I cover concepts relating to digital electronics. In this video I talk about state tables and ...

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**DVD - Lecture 3: Logic Synthesis - Part 1** Bar-Ilan University

83-612: Digital VLSI Design

This is Lecture 3 of the Digital VLSI Design course at Bar-Ilan University. In ...

**S-5 | Logic Synthesis of RTL in Synopsys Design Compiler**

**| RTL-to-GDSII flow | dc\_shell | DC Tutorial** This is the session-5 of RTL-to-GDSII flow series of video tutorial. In this session, we have demonstrated the synthesis flow ...

**Mealy and Moore State Machines (Part 1)** Digital

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**STA\_L1d - Importance of Timing From RTL to Logic Synthesis** To understand the importance of STA, it's very important to know VLSI Design flow and how different timing

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**Lecture 46: Synthesis of Sequential Logic Circuit: Moore Model and Mealy Model**

**DVD - Lecture 4: Logic Synthesis - Part II** Bar-Ilan University  
83-612: Digital VLSI Design

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**STA\_L1e -Timing Optimization During Logic Synthesis** To understand the importance of STA, it's very important to know

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VLSI Design flow and how different timing checks are required at ...

**Introduction to Synthesis** Advanced Logic Synthesis by Dhiraj Taneja, Broadcom, Hyderabad. For more details on NPTEL visit <http://nptel.ac.in>

**4.3(c) - Combinational Logic Synthesis: SOP Design Example**

**Multi-level Logic Synthesis: Technology Mapping**

**7.4(b) - FSM Synthesis**

**8-bit CPU control logic: Part 3** See

<https://eater.net/bbcpu8-control-logic> for more.

In this video we use two EEPROMs to translate the instruction

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